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(54) Title: ARRANGEMENT AND METHOD RELATING TO RADIO COMMUNICATION

(57) Abstract

The present invention relates to an arrangement (100) and a method respectively for suppressing clock overtones generated in a receiving arrangement of a radio communication system which receives signals within at least one frequency band and wherein the receiving arrangement comprises a number of oscillators including local oscillators and digital clocking means. The arrangement (100) comprises a phase locking arrangement (20) which includes a number of phase locking means (22; 23) for locking the oscillators in relation to each other so that all clock overtone frequencies become co-located and well defined within the frequency band(s). The arrangement further comprises a filtering arrangement (40) for filtering out said clock overtones, thus producing an output signal (I OUT/40) which is substantially free from clock overtones.

Title
ARRANGEMENT AND METHOD RELATING TO RADIO COMMUNICATION

5

FIELD OF THE INVENTION
The present invention relates to an arrangement and a method of suppressing clock overtones in a receiving arrangement of a radio communcation system.

10

The invention also relates to a receiving arrangement in a radio communication system receiving signals within at least one frequency band and in which clock overtones may be produced.

15   STATE OF THE ART
Modern radio receivers commonly use analogue as well as digital technique. Digital signals have a particular clock frequency and digital clocks always produce overtones, which are multiples of the fundamental frequency, leaking into the receiver itself.

20   Mostly it is attempted to shield sensitive parts within a receiving arrangement so as to prevent their being affected by the overtones. Furthermore the source, for example the digital clock itself, is shielded. Today, however, there is a need to be able to fabricate arrangements which are highly integrated and it is

25   therefore both cumbersome and expensive to provide for extensive shielding. Furthermore, shielding itself prevents the fabrication of arrangements which are as highly integrated as desired.

It is also known to use frequency planning to prevent overtones

30   from falling within the bandwidth of a receiving arrangement. This may be a good solution if the receiver works within a limited

frequency range, but if a broadband receiving arrangement is needed, or, if the same digital blocks are to be reused in different arrangements intended for different frequencies, frequency planning will simply not function. Today the same standard is often applied in different frequency bands and it is an advantage to be able to reuse the digital part of a construction whereas the radio frequent part is exchanged. Frequency planning will also not function since it is very difficult to find a set of oscillator frequencies for which no overtone or combination of overtones fall within the bandwidth(s) of the receiver, particularly if two frequency bands are used such as for example 800 and 1500 MHz.

SUMMARY OF THE INVENTION

What is needed is therefore an arrangement for suppressing clock overtones produced in a receiving arrangement including oscillators and digital clocks. An arrangement is also needed which allows a high degree of integration of involved components. Still further an arrangement is needed for suppressing clock overtones generated in a receiving arrangement of a radio communication system which is a broadband device or which operates in different frequency bands.

An arrangement for suppressing clock overtones is also needed allowing reuse of the digital part of the arrangement in different parts intended for different frequencies.

Particularly an arrangement is needed which enables suppression of clock overtones when the signal strength varies rapidly or when the amplitude varies rapidly and to a high extent. Particularly an arrangement is needed which enables the handling of the fast

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variations in signal strength that are produced in the input signal in a TDMA (time division multiple access) system. In such a system a number of users share one and the same frequency, i.e. a number of users are assigned one time slot each.

A receiving arrangement in a radio communication system is also needed through which the above mentioned objects are achieved as well a method of suppressing clock overtones in a receiving arrangement of a radio communication system through which the above mentioned objects are fulfilled.

Therefore an arrangement is provided which comprises a number of phase locking means for locking the oscillators which might produce a disturbing frequency in relation to each other or in relation to a reference clock so that all clock overtone frequencies are co-located and well defined within the frequency band. The arrangement also includes a filtering arrangement for filtering out said clock overtones so as to produce an output signal substantially free from clock overtones. Advantageously the filter arrangement comprises a narrow band digital filter. If the variation in amplitude of the signal is slow, the filtering arrangement advantageously comprises a high pass filter or a band reject filter which is applicable for example in an FDMA (frequency division multiple access system).

In an alternative embodiment, in case the variation in amplitude of the signal is fast, the filtering arrangement comprises a number of filtering means, each of which comprises a low pass filter or a bandpass filter for filtering of the input signal and signal adding means for subtracting the (low pass) filtered signal from the input signal. By input signal is here meant the signal

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input to the filtering arrangement which is output from the phase
locking means.

The filtering means particularly include comparing means for
5   comparing the absolute value of the input signal amplitude with a
given threshold value and the filter is inactivated if the signal
amplitude exceeds the given threshold value. The (low pass) filter
is advantageously advanced stepwise if the amplitude of the
received signal is below the threshold value. Advantageously the
10   (low pass) filter is a digital filter. In an advantageous
embodiment the comparing means operates using hystheresis. In that
way is avoided that, in a transition area, the signal modulation
makes the filter repeatedly alternate between an integrating and a
holding mode of operation. A low pass filter in combination with
15   signal adding means is advantageously used if the amplitude of the
input signal varies much and/or rapidly. Particularly the radio
communication system comprises a TDMA access system in which a
number of users share the same frequency, each user being assigned
a different time slot.
20

In a particular embodiment, instead of comparing the absolute
value of the input signal with a threshold value, separate filter
means (high pass filters or band reject filters) can be provided
for each time slot and time controlling means are provided
25   assigning one filter for the signal in each respective time slot
and for selecting an output signal from one of the filters, i.e.
selecting one of the filters as the active one to produce an
output signal.

30   Particularly the phase locking means comprises a number of phase
locked loops (PLLs). In a particular embodiment it is also

supposed that the disturbing signal has been transformed or converted to zero frequency by a preceding radio receiver in combination with the digital signal processing. After the disturbing signal has been suppressed, the useful signal can be converted to the desired frequency. In a particular embodiment, the frequencies in the system are so chosen that the second frequency conversion, i.e. the conversion of the useful frequency to a desired frequency, is not needed.

In a particularly advantageous embodiment, the arrangement is implemented as a digital application specific integrated circuit (ASIC).

A receiving arrangement for receiving signals within at least one frequency band is also provided. The receiving arrangement, in a conventional manner, comprises a number of oscillators, digital clocking means and mixing means for selecting a channel and converting down a received signal to base band or to an intermediate frequency. According to the invention the receiving arrangement comprises a number of phase locking means, particuarly phase locked loops (PLL) for locking the oscillating means and the digital clocking means in relation to each other so that all generated disturbing frequencies are co-located and well defined within the frequency band(s). A filtering arrangement, particularly a narrow filter, is used for filtering out the disturbing frequencies.

In a particular embodiment the receiving arrangement is used in a TDMA system in which a number of users share one and the same frequency in that one time slot is assigned for each user. This may produce a considerable variation in signal amplitude from one

time slot to another, and to handle this particular situation, or more generally a situation in which the signal amplitude varies rapidly or to a high extent, the filtering arrangement includes a bandpass filter, or particularly a low-pass filter (if the signal

5   has been converted to zero frequency) for filtering of the received signal which is input to the filtering arrangement after the frequencies have been locked in relation to each other. The filtering arrangement also includes signal adding means for subtracting the filtered signal from the input signal. Still more

10   particularly the filtering means includes comparing means for comparing the absolute value of the input signal amplitude with a given threshold value and the filtering means is activated if the signal amplitude exceeds the given threshold value. If the amplitude of the received signal is below the threshold value, the

15   bandpass filter (or the low-pass filter) is advanced stepwise. Alternatively, as referred to above relating to the the arrangement of suppressing clock overtones, a number of band reject or highpass filters can be provided, controlling means being provided using a time base for time control and for

20   selecting one of the filter means to be the active one through a clock enable signal and using the signal from the active filter as output data.

A method of suppressing clock overtones generated or produced in a

25   receiving arrangement of a radio communication system is also disclosed which includes the steps of: locking all oscillating means and digital clocks that might produce a disturbing frequency to each other or to a predetermined reference clock so that the frequencies are co-located and well defined within the frequency

30   band and using a filter arrangement to filter out the co-located and well defined disturbing frequencies. Particularly the method

is applied on a signal which varies rapidly, or to a high extent, in amplitude such as for example in a TDMA access system. The absolute value of a received and a selected signal is then taken. The received signal, i.e. the absolute value of its amplitude, is

5   in comparing means compared with a given threshold value, and, if the signal amplitude is lower than the given threshold value, a bandpass or a low-pass filter is advanced stepwise, otherwise the value is maintained. The signal is then passed through the filter and the filtered signal is subtracted from the input, or the

10 received, signal to provide an output signal thus being the difference between the input signal and the filtered signal. As referred to earlier, instead of using a threshold value, a number of filter means can be provided each e.g. for the signal in a particular time slot, in which case the filters comprise band

15 reject filters (high pass filters).

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will in the following be further described in a non-
limiting manner and with reference to the accompanying drawings,
in which:

5

FIG 1   shows a simplified filtering arrangement according to a
            first embodiment of the invention in which the amplitude
            of the input signal varies slowly,

FIG 2a   shows an input signal having a fast variation in signal
10   strength,

FIG 2b   shows the output signal for an input signal as in Fig 2a
            if an arrangement according to the embodiment of Fig 1
            is used,

FIG 3   shows an alternative embodiment of a filtering
15   arrangement according to the invention for an input
            signal having a fast variation in signal strength,

FIG 4   shows an embodiment similar to that of Fig 3 in which
            automatic gain control is implemented,

FIG 5   shows an example on a phase locked loop (PLL),

20 FIG 6   shows a phase locking arrangement according to the
            invention which comprises two phase locked loops,

FIG 7   shows an alternative embodiment of a filtering
            arrangement using a number of filters, one for each time
            slot in a TDMA system, and

25 FIG 8   is a simplified flow diagram relating to suppressing of
            clock overtones according to one embodiment of the
            invention.

DETAILED DESCRIPTION OF THE INVENTION

30 According to the invention all oscillators, i.e. all oscillating
    means such as local oscillators and digital clocks are phase

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locked for example using PLL:s as further discussed under reference to Figs 5 and 6 so that all potential disturbing frequencies are well defined within the frequency band. The disturing frequencies are filtered out through the use of a

5   filter, for example a narrow digital filter. If the arrangement is used in a system in which the variation in signal amplitude is comparatively slow, for example a FDMA (frequency division multiple access) system, a high pass filter, or more generally, a band reject filter can be used.

10

If however, the signal amplitude varies more rapidly, such as for example the input signal in a TDMA system, a bandpass filter or particularly a low pass filter is used and the difference is taken between the filtered input signal and the input signal. Such a

15   filter arrangement 30 is schematically illustrated in Fig. 1. Input signal I_{30}^{IN}, received from a phase locking arrangement, (i.e. the frequencies of oscillators, digital clocks are locked to each other enabling filtering out of disturbing frequencies), is filtered in bandpass (low pass) filter 33. In adding means 34 the

20   filtered signal I_{30}^{f} is subtracted from the input signal I_{30}^{IN}. However, in this filter arrangement 30 a threshold value is set which is so high that the filter 33 always is active. In the following it is supposed that the disturbing signal has been converted to zero frequency by a preceding radio receiver in

25   combination with digital signal processing. As already referred to earlier in the application, this has in no way a limiting effect on the applicability of the inventive concept since, after suppression of the disturbing frequencies, the useful signal can be converted to the wanted frequency. In a particular embodiment

30   the frequencies used in the system are so chosen that there is no

10

need to convert the useful signal. In order to suppress a DC component of a received signal a high pass filter having a limiting frequency (threshold frequency) which is so low that the useful signal is not affected considerably can be used (if the
5   signal strength varies slowly). The limiting frequency must at the same time be sufficiently high to suppress the undesired low frequency component.

In general there can be said to be three different cases. In the
10   first case as already discussed above, the disturbing frequency is already at zero frequency (as well as the frequency of the useful signal). Then a lowpass filter is used and the disturbing signal is subtracted from the useful signal.

15   In a second case the center frequency of the useful signal is not zero and a conversion is performed so that the disturbing frequency is converted to zero. Then a lowpass filter as discussed above can be used but when the disturbing frequency has been subtracted, the signal has to be converted to zero frequency.
20
Finally the useful frequency can be centered around zero but not the disturbing frequency. Then a bandpass filter is used to give the disturbing frequency. The disturbing frequency is then subtracted from the signal in any convenient manner.
25
In a TDMA system the variation in received signal strength between different users can vary a lot. This means that, when there is a change from a strong signal to a weak signal, the remaining imbalance from the strong signal will not have time to fade out
30   before reception of the weak signal starts. This makes the reception of the weak signal poor or even impossible. This will in

the following be further described under reference to Figs. 2a and 2b. If the signal in one time slot (each user is assigned a particular time slot) is strong, whereas signals of the other time slots are weak, is schematically illustrated in Fig. 2a which is a
5   simplified illustration showing an input signal I_{30}^{IN} comprising one TDMA-frame with three time slots per carrier frequency, time slots TS 1, 2 and 3, the signal in time slot 1 being strong. The low-pass filtered signal I_{30}^{f} will then be as in Fig. 2b. The remaining imbalance from the signal in time slot 1 will disturb time slot 2
10   if its level is not well below the noise floor. Through inactivating the filter for strong signals, the remaining disturbance will be prevented from being too high. If for example a threshold value of 20dB above the noise level is used, and the signal is suppressed 30dB in the filter, the disturbing signal
15   will be eliminated whereas the "tail" will be about 10dB below the noise level and it will thus not disturb the weak signals, e.g. the signal from time slot 2.

In Fig. 3 an arrangement for suppressing a low frequency signal
20   component is illustrated. An input signal I_{40}^{IN} is provided, (from a phase locking arrangement), for example an input signal of a TDMA system with a fast variation in amplitude. Means 41 are provided for taking the absolute value of the amplitude of the input signal I_{40}^{IN}. The input signal is either real or complex. If the input
25   signal is a complex signal, an approximation of the absolute value is given through integrating over the absolute value of the quadrature components, $\left(\sqrt{I^2 + Q^2} \approx |I| + |Q| \right)$. In comparing means 42 the absolute value is compared with a given threshold value

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THR. If the absolute value of the signal is below the threshold value, the low-pass filter 43 is advanced stepwise and if the absolute value is above the threshold, the preceding value is kept. In adding means 44 the low-pass filtered signal I_{40}^{LP} is

5   subtracted from the input signal I_{40}^{IN} providing an output signal I_{40}^{out}. The signal output from the low-pass filter 43 is only affected when the total amplitude is small and therefore a long time constant can be used in such a filter still preventing a strong input signal from creating any residues in the filter.

10

In an advantageous embodiment the comparing means 42 uses a hystheresis. Within a transition area it is then prevented that the modulation of the signal makes the filter repeatedly alternate between an integrating and a holding state.

15

The bandwidth of the low-pass filter is chosen to be sufficiently small so as to only have a neglectable effect on the useful signal but it still has to be large enough so as to suppress the disturbing signal which, because of phase noise of the oscillators

20   in the system, may have a certain bandwidth.

In the arrangement of Fig. 3, it is supposed that the disturbing signal generally has the character of a leaking signal and in that it is small as compared to the available width of signal.

25

In Fig. 4 a filtering arrangement 50 similar to that of Fig. 3 is illustrated but in which automatic gain control (AGC) is applied.

In general it is difficult to find a set of oscillator frequencies

30   for which no overtone, or combination of overtones fall within the

13

bandwidth of the receiver. A particular case is when both the 800 and the 1500 MHz frequency bands are considered. Supposing a channel separation of 25 kHz, c.f. for example the PDC-standard (Pacific Digital Cellular) communication system. If a sampling

5   frequency of 4.2 MHz is used, which is a multiple of 25 kHz, the overtones from the sampling clock will always be converted down to zero frequency. If local oscillators and transmitting oscillators are locked to also be multiples of 25 kHz all the mixing products are converted down to zero frequency. With a high-pass filter with

10 a low cut-off frequency, such a component can be suppressed. If the same reference is used both for the sampling clock and the local oscillators, the filter can have a cut-off frequency determined only by the width of the leakage signal or the disturbing signal. If however, the reference frequency from a

15 first local oscillator and the sampling frequency come from different sources, a non-zero bandwidth is requried. According to the invention a recursive filter can be used (of course also other filter types can be used), for which the cut-off frequency can be low enough so as not to produce any phase shift of the wanted

20 signal. If the system is TDMA based, as referred to above, there may be a very large difference of the signal amplitude between adjacent time slots and a switch from a strong signal to a weak signal near the sensitivity level, where the DC suppression is intended to be of use, will cause the residual effect from any

25 imperfections in the signal distribution in the I/Q-plane to disrupt the signal output. In the embodiment as shown in Fig. 4 automatic gain control (AGC) is applied which also may produce a varying DC level in the filter. The filtering arrangement 50 also in this case comprises means 51 for taking the absolute value of

30 the signal, comparing means 52 and a low-pass filter 53 and adding means 54 in which the difference is taken between the input signal

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I_{50}^{IN} and the low-pass filtered signal I_{50}^{LP}. The low-pass filter 53 is only advanced if the absolute value of the signal level is below a certain threshold value. In this way a strong signal does not create any residues in the filter. If the automatic gain

5 control is active (not maximum gain), the filter is not used at all in this particular embodiment and switches 55,56 are used through which the filter is "disconnected/connected". This embodiment substantially corresponds to that of Fig. 3, it is merely intended to show that AGC can be implemented and that AGC

10 may produce additional disturbances having to be handled. If the gain control (AGC) is used, e.g. if the gain is controlled, this generally means that the signal is quite strong, and then the filtering functionality may have to be disconnected as illustrated through the switches.

15

In Fig. 5 a block diagram of a phase locked loop (PLL) 10 is schematically illustrated, a number of which PLL:s · can be implemented in the phase locking arrangement as referred to in the foregoing. A signal I_{REF} giving the time base, i.e. the reference

20 frequency is in dividing means 12 divided by a factor N. The VCO-signal (to be locked) having a frequency f_{OUT} is divided by a factor M in dividing means 13. A phase detector 14 gives an output signal with pulses having a width which is proportional to the phase difference between the two divided signals. The signal is

25 then filtered in the loop filter 15 and fed back as a control signal to the VCO to minimize the error of the signal from the loop filter which is proprtional to the error in phase. The output signal f_{OUT} will then have a fixed relation to the input signal I^{REF} as $f_{OUT}/M = I_{10}^{REF}/N$. Through changing M and N, f_{OUT} can be controlled

30 and used for example to set a channel. This PLL 10 is however only

one simple example of a PLL that can be used. Many other kinds of PLL:s can of course also be used.

In Fig. 6 an arrangement 100 according to the invention comprising
5   a locking arrangement 20 with two phase locking means 22,23 for locking the oscillating means and the digital clocking means in relation to the reference oscillator 21 and to each other and a filtering arrangement 40 as disclosed in Fig. 3 is illustrated. The reference oscillator 21 generates an input signal with the
10 reference frequency I^{REF}_{20}. A channel selection is carried out through setting $f_{23}=f_{RX}$, f_{22} being the frequency of the local oscillator 23 and f_{RX} being the frequency of the input signal I_{RX}. The signal will then be converted to zero frequency in the mixer 25. An RF-filter 24 is implemented in the receiving arrangement in
15 a conventional manner. Δf is the bandwidth of the input signal I_{RX} divided by two. For some channel $f_{RX}-\Delta f<kxf_{22}<f_{RX}+\Delta f$. The simplest case is $kxf_{22}=f_{RX}(=f_{23})$. This disturbing signal having this frequency will also ·be mixed and converted to zero frequency. If PLL1 22 had not been locked to the same reference frequency as
20 PLL2 23, kxf_{22} whould. have been approximately the same as f_{RX} with a tolerence of some ppm (typically about 100). Using locking according to the invention, f_{22} and f_{23} will be locked to each other so that filtering with the filtering arrangement 40 as described with reference to Fig. 3 is enabled. The filtering will
25 therefore not be further described here.

It should however be clear that a receiving arrangement generally comprises several filters, mixers, amplifiers etc. but this is not further discussed herein, since it is supposed to be well known to
30 the person skilled in the art how a receiving arrangement can be built.

16

In Fig. 7 an alternative embodiment of a filtering arrangement 60
is illustrated. It is supposed that all oscillators are locked to
each other (or rather to a reference frequency) in any convenient
5   manner, for example as discussed with reference to Fig. 6. This
arrangement is also applicable to a receiving arrangement in a
TDMA based system or more generally in a system in which an input
signal varies much or rapidly in amplitude. In this case it is
supposed however, that it is a TDMA based system used in GSM in
10   which 8 users share one and the same frequency, one time slot
being assinged for each user. For example in ADC or PDC (American
Digital Cellular or Pacific Digital Cellular communication systems
there are instead of eight, three time slots in a TDMA frame. In
the arrangement 60 there is one high pass (or band reject) filter
15   61-68 for each of the eight time slots. In this case no setting of
threshold values is needed. Instead a time base is used for
controlling in controlling means 69A. Through controlling the
clocking of each filter 61-68 it is possible to make every filter
just seeing e.g. the signal in one particular assigned time slot
20   respectively. Through the controlling means 69A one of the filters
is enabled or selected to be active, and in the illustrated
embodiment it is the second filter means 62. As output data the
signal I_{62}^{out} from the selected filter 62 is provided from the
multiplexer 69B. For the functioning of this arrangement it is
25   supposed that the limits of the time slots can be predicted with
sufficient accuracy. That in Fig. 7 eight filter means are
illustrated corresponding to eight time slots as used in for
example the GSM system, is merely given as an example for
illustrative purposes.

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The input signal I_{60}^{IN} received in receiving arrangement 60 is a signal output from a locking arrangement, e.g. as disclosed in Fig. 6.

5   In Fig. 8 a flow diagram relating to one particular embodiment is schematically illustrated. In a first step all oscillators and digital clocks are locked in relation to each other or in relation to a reference (which also inherently means that they are locked to each other), 110. All is here taken to mean all

10 oscillators/digital clocks which might produce a disturbing frequency or clock overtones. The locking as such is not described so carefully since it can be done in different ways. The important aspect is that locking actually is provided for, e.g. using PLL:s instead of freely oscillating oscillators as in hitherto known

15 arrangements used for the same purpose, which does not permit any filtering out of disturbing frequencies. Filtering is then, according to the invention, performed using any of the arrangements described herein. A locked signal is thus received in a filtering arrangement, 120. In an embodiment as illustrated

20 through this flow diagram, a predetermined threshold value is used. The absolute value of the signal amplitude is then calculated, 130, as discussed earlier in the application and after that the absolute value of the signal amplitude is compared in comparing means with the given threshold value, 140. If the

25 absolute value of the amplitude exceeds the threshold value, 150, the filter value is kept, 160. If, on the other hand, the absolute value of the signal amplitude is lower than the threshold value, the filter is advanced stepwise, 151. The signal is then passed through the low-pass filter, 170, and provided to adding means in

30 which the low-pass filtered signal is subtracted from the received

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signal, 180. The signal so obtained is then ouput, 190. Of course, as referred to earlier in the application, more generally a band pass filter is used.

5   It should be clear that the invention is not limited to the illustrated embodiments but it can be varied in a number of ways within the scope of the appended claims. Particularly different filtering arrangements can be combined with different phase locking arrangements to filter out disturbing frequencies.

10

CLAIMS

1. Arrangement (100) of suppressing clock overtones generated in a
receiving arrangement of a radio communication system for
receiving signals within at least one frequency band, said
receiving arrangement comprising a number of oscillators including
local oscillators and digital clocking means,
c h a r a c t e r i z e d   i n
that it comprises a phase locking arrangement including a number
of phase locking means (10;20) for locking the oscillators in
relation to each other so that all clock overtone frequencies are
co-located and well defined within the frequency band(s), and a
filtering arrangement (30;40;50;60) for filtering out of said
clock overtones, thus producing an output signal I_{40}^{out}, I_{50}^{out}, I_{62}^{out}
substantially free from clock overtones.

2. Arrangement according to claim 1,
c h a r a c t e r i z e d   i n
that the variation in amplitude of the received signal is slow and
in that the filtering arrangement (30;40;50;60) comprises at least
one band reject filter or high pass filter.

3. Arrangement according to claim 1,
c h a r a c t e r i z e d   i n
that the variation in amplitude of a received signal is fast and
in that the filtering arrangement comprises a number of filter
means, each comprising at least one bandpass filter or lowpass
filter (33;43;53) for filtering the received signal and signal

20

adding means (34;44;54) for subtracting the filtered signal from
the received signal.

4. Arrangement according to claim 3,
5   c h a r a c t e r i z e d   i n
that the filtering means includes comparing means (42;52) for
comparing the absolute value of the received signal amplitude with
a given threshold value (THR) and in that the filter is
inactivated if the signal amplitude exceeds the given threshold
10   value.

5. Arrangement according to claim 4,
c h a r a c t e r i z e d   i n
that the bandpass filter or particularly the lowpass filter
15   (33;43;53) is advanced stepwise if the amplitude of the received
signal is below the threshold value.

6. Arrangement according to any one of claims 2-5,
c h a r a c t e r i z e d   i n
20   that the filtering arrangement comprises (a) digital filter(s).

7. Arrangement according to any one of claims 4-6,
c h a r a c t e r i z e d   i n
that the comparing means (42;52) operate using hystheresis.

25

8. Arrangement according to any one of claims 3-7,
c h a r a c t e r i z e d   i n
that the amplitude of the received signal varies much and/or
rapidly.

30

9. Arrangement according to claim 8,

c h a r a c t e r i z e d   i n
that the radio communication system comprises a TDMA access system
in which a number of users share the same frequency, each user
being assigned a different time slot.

10. Arrangement according to claim 3,
c h a r a c t e r i z e d   i n
that the radio communication system comprises a TDMA access system
in which a number of users share the same frequency, each user
being assigned a different time slot and in that separate filter
means (61,...,68) are provided for each time slot and in that time
controlling means (69A) are provided assigning one filter for the
signal in one time slot respectively and for selecting an output
signal (I_{62}^{out}) from one of the filters (62) through activating one
of the filters (62).

11. Arrangement according to any one of the preceding claims,
c h a r a c t e r i z e d   i n
that each phase locking means comprises a phase locked loop (PLL)
and in that the local oscillators comprise voltage controlled
oscillators (VCO).

12. Arrangement according to claim 9, 10 or 11,
c h a r a c t e r i z e d   i n
that it furthermore comprises frequency converting means for
converting down the frequency of the received signal to zero
frequency.

13. Arrangement according to claim 2,
c h a r a c t e r i z e d   i n

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that the radio communication system comprises a CDMA or a FDMA access system.

14. Arrangement according to any one of the preceding claims,
5   c h a r a c t e r i z e d   i n
that it is implemented as a digital application specific integrated circuit (ASIC).

15. Arrangement according to any one of the preceding claims,
10   c h a r a c t e r i z e d   i n
that second converting means are provided for converting the output signal to a desired frequency.

16. Receiving arrangement in a radio communication system for
15   receiving signals within at least one frequency band, comprising oscillating means, digital clocking means and mixing means for selecting a channel and converting down the received, selected signal to base band or to an intermediate frequency,
c h a r a c t e r i z e d   i n
20   that it comprises a number of phase locking means (10;20) for locking the oscillating means and the digital clocking means in relation to each other so that all generated disturbing frequencies are co-located and well defined, and a filtering arrangement (30;40;50;60) for filtering out the disturbing
25   frequencies.

17. Receiving arrangement according to claim 16,
c h a r a c t e r i z e d   i n
that a number of users share the same frequency, one time slot
30   being assigned for each user (TDMA) so that the signal amplitude may vary considerably from time slot to time slot, and in that the

filtering arrangement comprises at least one bandpass filter,
particularly a low pass filter (33;43;53) for filtering the
received signal and signal adding means (34;44;54) for
substracting the filtered signal from the received signal.

5

18. Receiving arrangement according to claim 17,
c h a r a c t e r i z e d   i n
that the filtering means includes comparing means (42;52) for
comparing the absolute value of the received signal amplitude with
10   a given treshold value and in that the filter is inactivated if
the signal amplitude exceeds the given threshold value.

19. Receiving arrangement according to claim 18,
c h a r a c t e r i z e d   i n
15   that the low pass filter is advanced stepwise if the amplitude of
the received signal is below the threshold value.

20. Method of suppressing clock overtones generated by oscillating
means or digital clocks in a receiving arrangement of a radio
20   communication system including a number of receiving arrangements,
c h a r a c t e r i z e d   i n
that it comprises the steps of:
    - locking all oscillating means and digital clocks able to produce
       a disturbing frequency to each other or to a predetermined
25   reference clock so that the frequencies are co-located and well
       defined,
    - using a filter arrangement (30;40;50;60) to filter out the co-
       located and well defined disturbing frequencies.

24

21. Method according to claim 20 wherein a TDMA access system is used, a number of users being assigned different time slots of one and the same frequency band (carrier frequency),
c h a r a c t e r i z e d   i n
5   that it comprises the steps of:
- taking the absolute value of a received and selected signal,
- comparing the received signal with a given threshold value,
- if the signal amplitude is lower than the given threshold value, advancing a bandpass or a low pass filter (33;43;53)
10   stepwise, otherwise maintaining the value,
- filtering the signal,
- subtracting the filtered signal from the input signal to provide an output signal.

15   22. Method according to claim 20 for use in a TDMA system wherein a number of users are assigned different time slots of one and the same frequency band,
c h a r a c t e r i z e d   i n
that it comprises the steps of:
20   - in the filtering arrangement assigning one high pass or band reject filter (61,...,68) to each time slot,
- clocking the filters so that each filter only acts the signal in the time slot to which it is assigned,
- activating one of the filters using controlling means (69A),
25   - providing an output (I^{out}_{62}) signal from the activated filter (62).

Fig. 1

Fig. 2a

Fig. 2b

Fig.3

Fig.4

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Fig.5

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Fig. 6

Fig.7

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Fig.8

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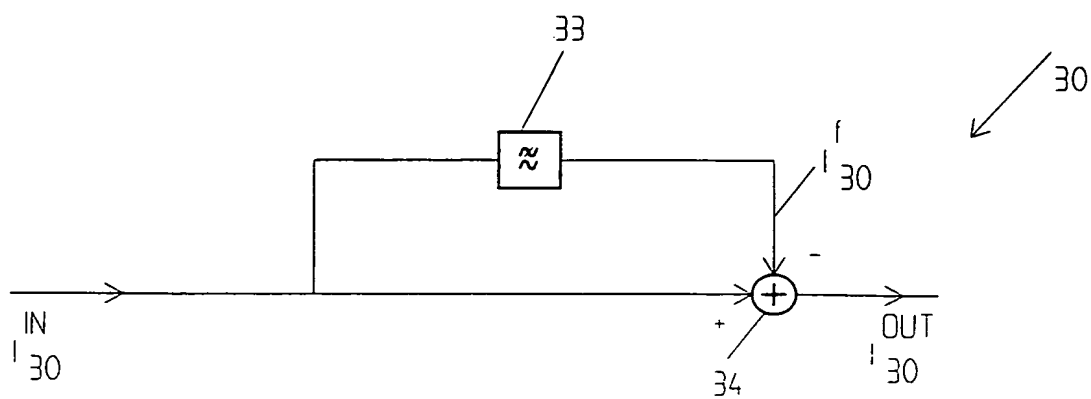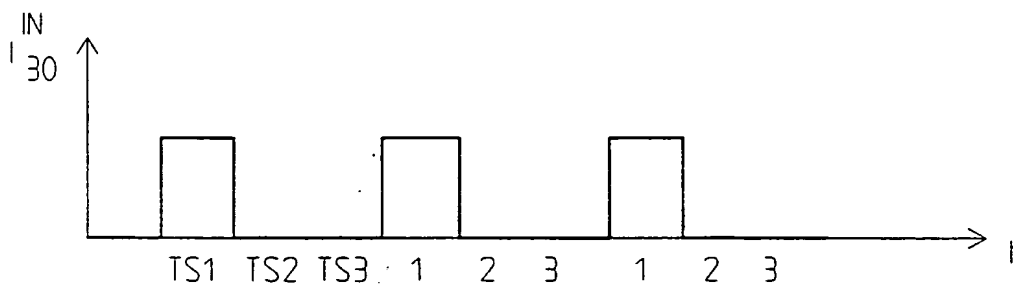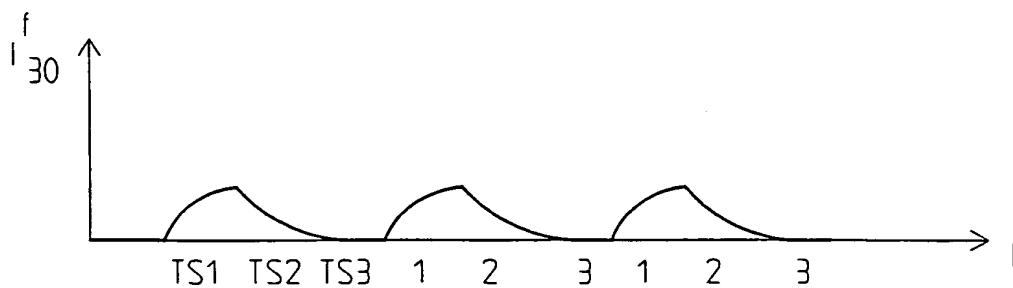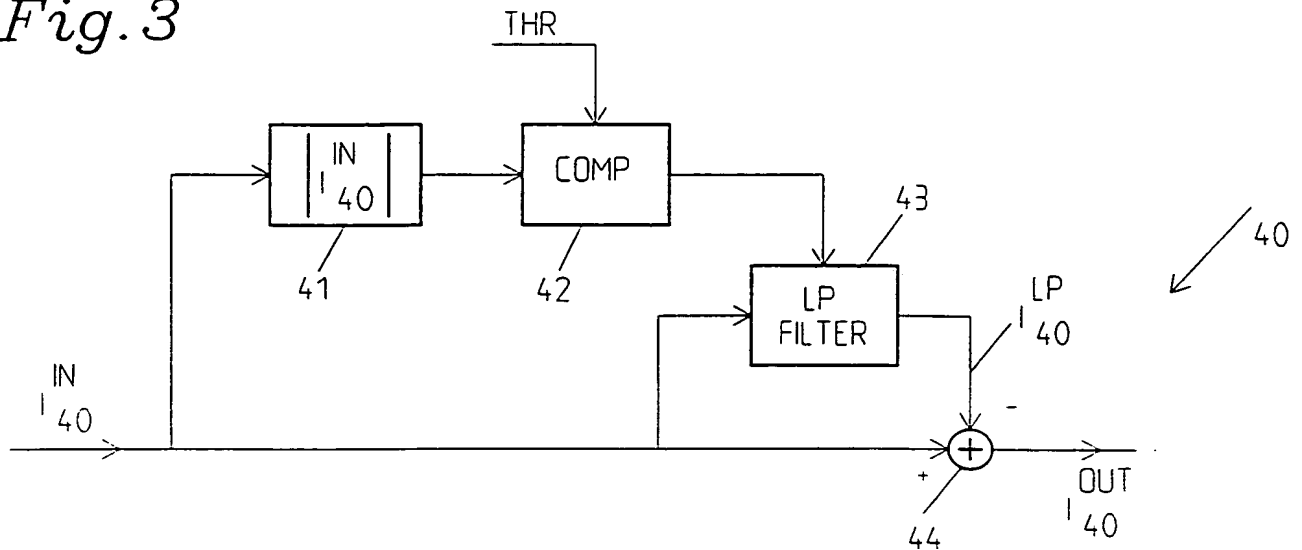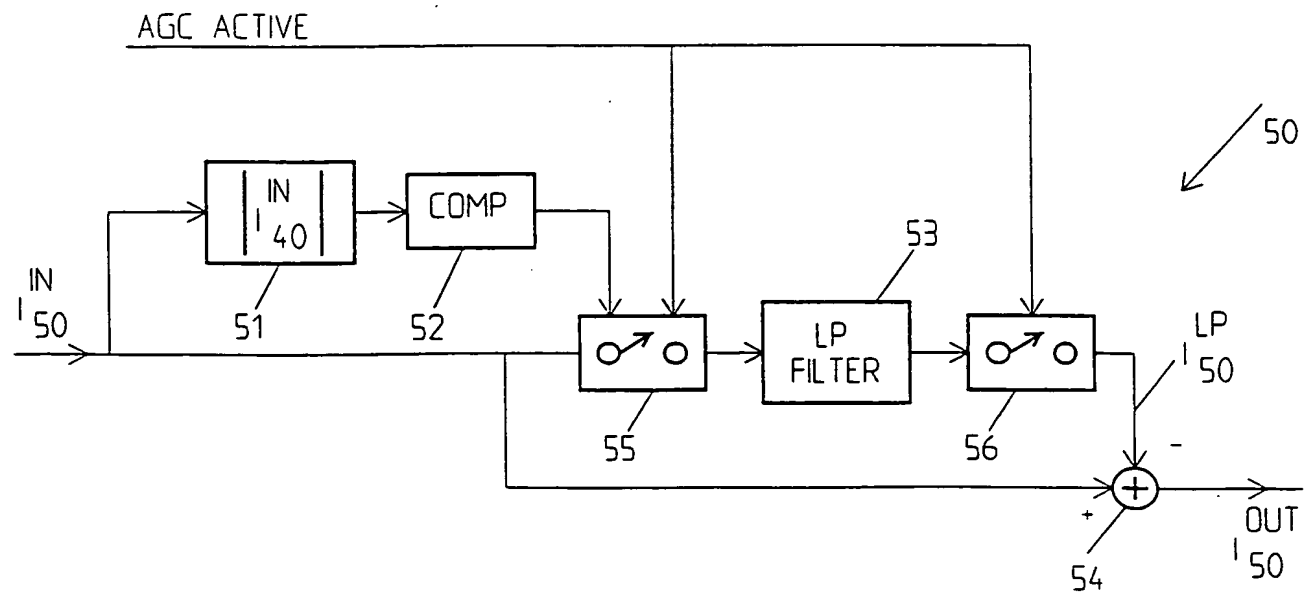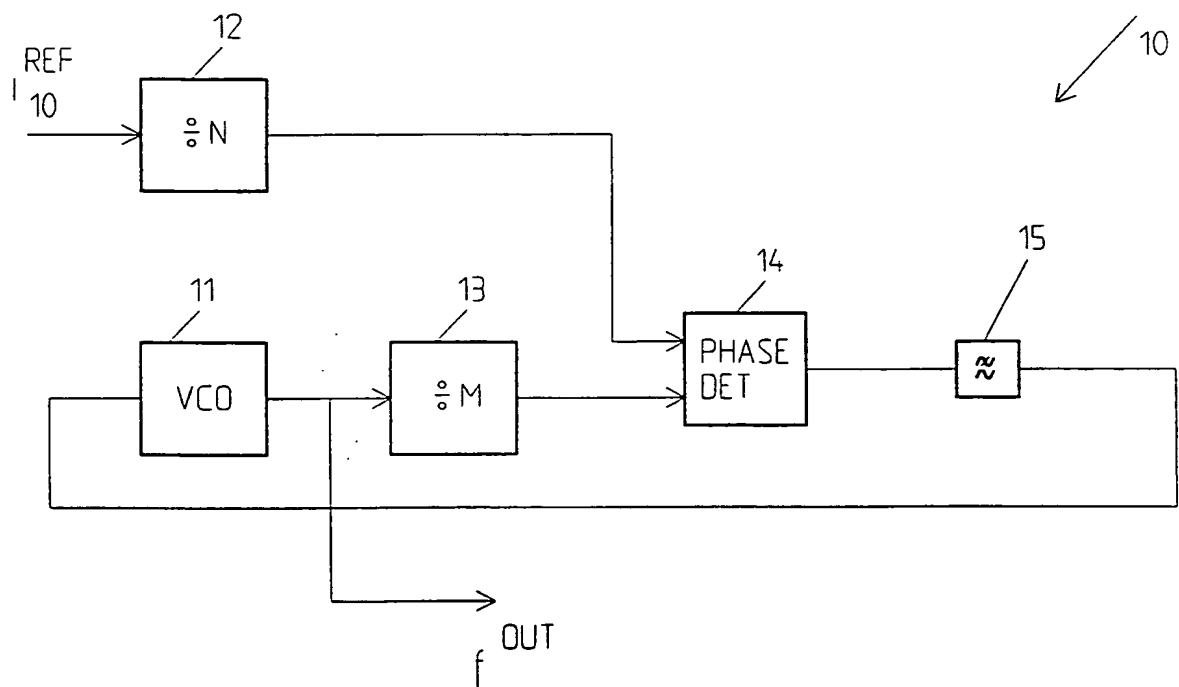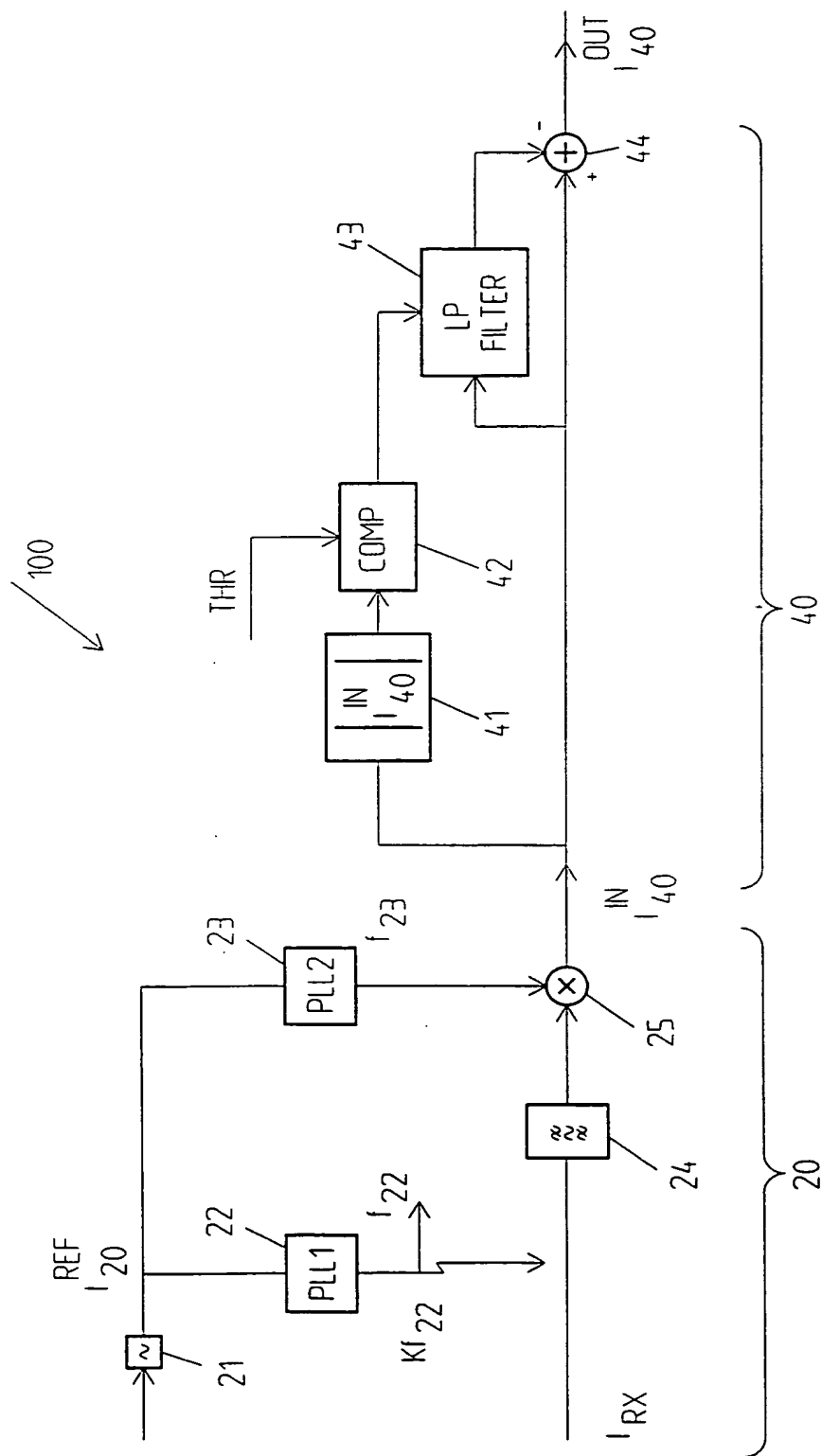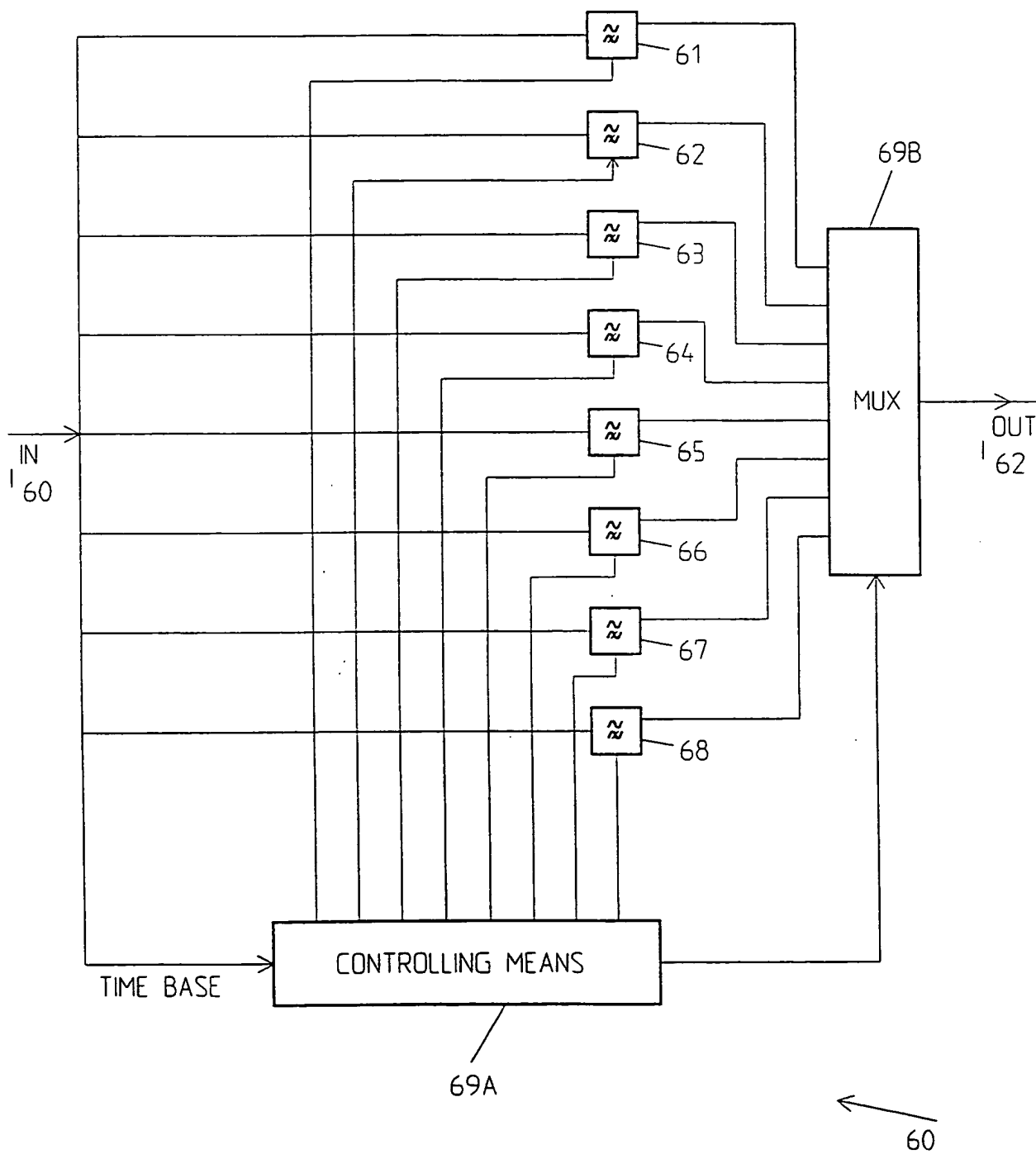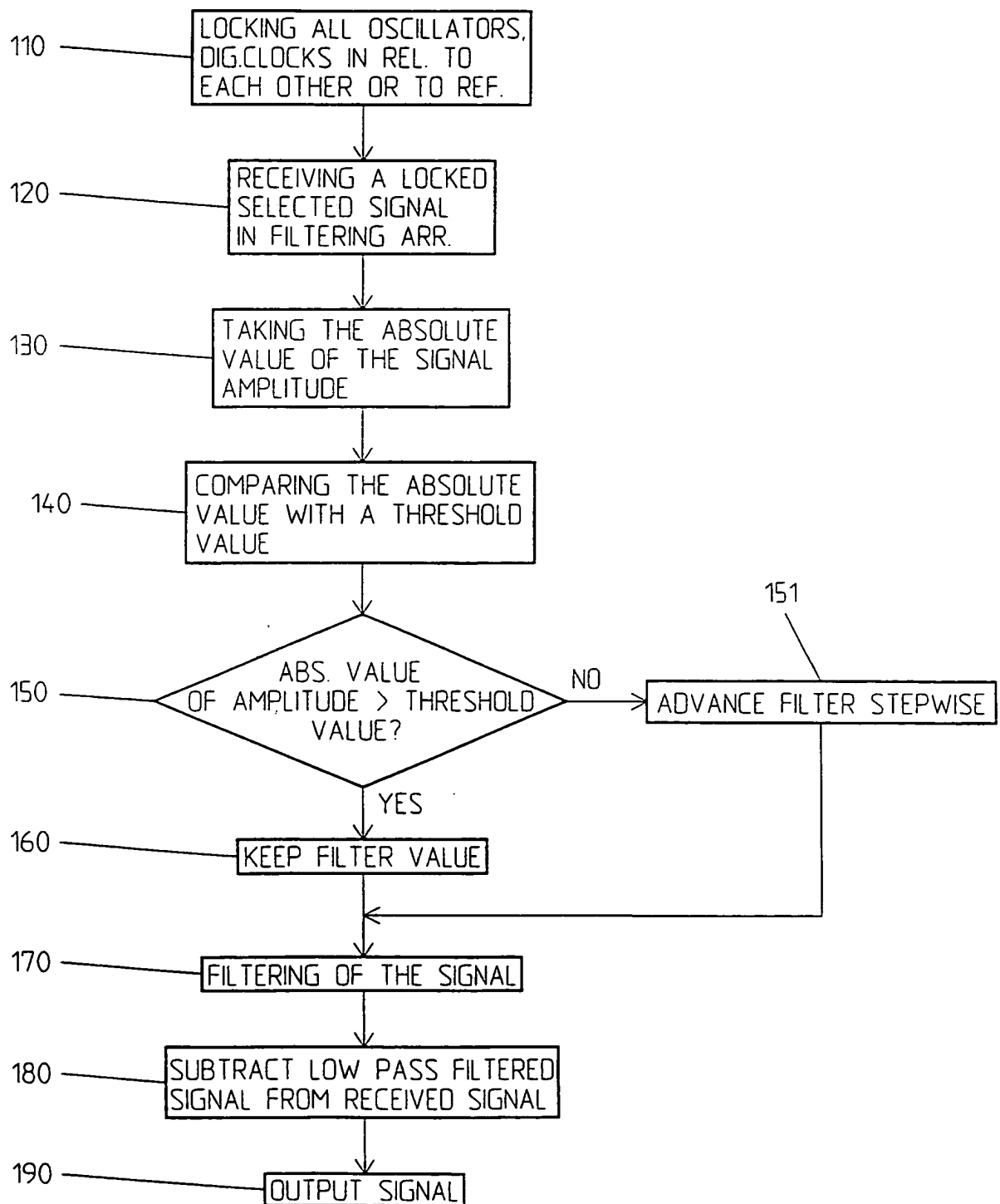
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(57) Abstract

The present invention relates to an arrangement (100) and a method respectively for suppressing clock overtones generated in a receiving arrangement of a radio communication system which receives signals within at least one frequency band and wherein the receiving arrangement comprises a number of oscillators including local oscillators and digital clocking means. The arrangement (100) comprises a phase locking arrangement (20) which includes a number of phase locking means (22; 23) for locking the oscillators in relation to each other so that all clock overtone frequencies become co–located and well defined within the frequency band(s). The arrangement further comprises a filtering arrangement (40) for filtering out said clock overtones, thus producing an output signal (I OUT/40) which is substantially free from clock overtones.

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04B 1/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04B, H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPIL, EDOC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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